A PRODUCIBLE 2 to 20 GHz MONOLITHIC POWER AMPLIFIER

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ABSTRACT

The design, fabrication, and performance of a 0.4-W, 2 to 20 GHz distributed amplifier are described in this paper. Small-signal gain is 5 dB and power-added efficiency is 15%. The amplifier is fabricated on ion-implanted GaAs, and achieves excellent performance through use of series gate capacitors and a tapered drain line. Circuit layout and optimization to obtain process insensitivity and first-pass design success are discussed. A comparison is made to a commercially available state-of-the-art 6 to 18 GHz amplifier designed using conventional (lossy-mismatch) topology. The distributed amplifier is shown to have much improved bandwidth, SWR, gain flatness, and insensitivity to process variations, while retaining similar output power and efficiency.

INTRODUCTION

There is an increasing demand for ultra-broadband amplifiers with power levels approaching 0.5 W. Distributed amplifiers have demonstrated very wideband performance, low gain ripple, and excellent input/output SWR. This paper describes a 0.4 watt, 2 to 20 GHz distributed amplifier with 5 dB gain and 15% power-added efficiency. The amplifier is fabricated on ion-implanted GaAs, and achieves excellent performance through use of series gate capacitors and a tapered drain line. Circuit layout and optimization to obtain process insensitivity and first-pass design success are discussed.

CIRCUIT DESIGN

The 2 to 20 GHz distributed power amplifier, designated TGA8220, uses six 335 µm FETs for a total gate width of 2010 µm. The design was based on conventional distributed amplifier synthesis which consists of coupling the input and output circuits of the active elements by means of an input and output artificial transmission line. The characteristic impedance is determined by the reactances associated with each device and by the interconnecting microstrip transmission lines.

To obtain the desired output power several non-conventional design techniques were used. The input capacitance associated with the large FET gate width of each stage reduces the cutoff frequency of the gate line. MIM capacitors were inserted in series with each FET, thus reducing the effective shunt capacitance on the artificial transmission line and extending the cut-off frequency [1]. The series capacitors and the FET input capacitance form a voltage divider to ground. The gate line MIM capacitors can be used to equalize the FET voltages along the line, resulting in significantly higher output power and efficiency for the amplifier. Figure 1 shows the drive levels predicted for the TGA8220 with the series tapered capacitors. These voltage levels were optimized on SuperCOMPACT.

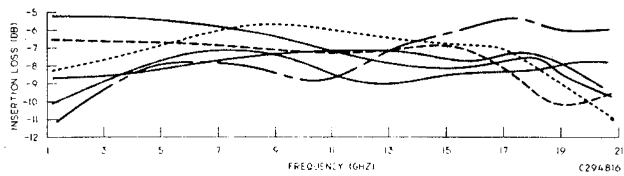

Figure 1. TGA8220 Gate Signals

The drain line impedance tapering scheme described in [1] was used to increase output power. The tapered line approach reduces the power loss in the termination; there is a cancellation of backward flowing current at each junction for characteristic impedance equal to Z_0/n, where Z_0 is the characteristic impedance of the first stage and n is the number of the stage of interest. Since the implementation of the precise tapering is impossible with the realizable microstrip range, the microstrip lines were linearly tapered from 60 to 100 ohms. The drain terminating resistor was made much higher than 50 ohms (230 ohms) to reduce power dissipation in the termination. It was also determined that the output power could be slightly increased by completely eliminating the drain termination, with negligible degradation of output match. The large FETs with low drain-source resistance provided enough loss to maintain a good output SWR.

Figure 2 is a photograph of the TGA8220 distributed amplifier. Circuit layout required consideration of several conflicting requirements. To minimize cost, total chip area should obviously be minimized. Only those microstrip discontinuities that

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were well modeled or had measured data available were used. For ease of integration into high-level assemblies, the RF inputs and outputs are in line and a DC block is included at the input port. Finished size of the TGA8220 is 131 x 74 mils, for a total of 663 chips per 3-inch wafer.

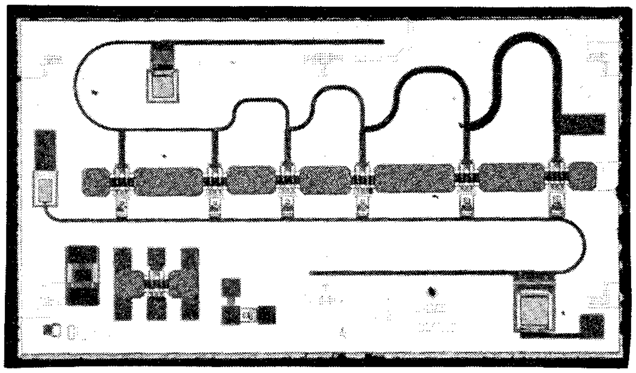


Figure 2. TGA8220 Amplifier

Drain bias for the TGA8220 is applied at the output end of the drain artificial transmission line. The last inductive section (connecting devices 5 and 6) must carry 5/6 of the total device current, the preceding section 2/3, and so forth until the first section (connecting devices 1 and 2) carries only 1/6 of the current. Current density in the drain transmission lines was carefully checked for conformance to design guidelines. Operating current density in the TGA8220 drain circuit is 0.1×10^6 A/cm^2.

Using series gate capacitors to raise the operating power level of the amplifier necessitates a parallel resistor for applying DC bias to the device gates. On the TGA8220, these resistors are located under the air-bridge connection from the gate artificial transmission line to the capacitor top plates. This configuration allows for simpler modeling. The 900-ohm resistor value is a compromise between physical resistor length (primarily constrained by airbridge inductance) and amplifier low-frequency gain flatness (when resistor conductance approaches that of the capacitor, gain peaking at low frequency will occur).

FABRICATION

Since 1982 the TI production facility has worked strictly with ion-implanted wafers. Ion implantation offers several production advantages, including high volume throughput, uniformity, and repeatability. The TGA8220 uses an "intermediate" implant profile, optimized for high power and gain. FET gate lengths are 0.5 µm; electron-beam lithography is used to define the TiPtAu gates. Ohmic contact metallization is AuGeNiAu, and MIM capacitors are constructed with 2000 Å thick silicon nitride (300 pF/mm^2). Transmission lines are plated to a total thickness of 5 µm to help reduce current density. At backside processing, substrate thickness is ground to 0.006", vias are formed by reactive ion etching (RIE), and backside gold is plated to a thickness of approximately 15 µm. Many of the process steps are totally automated, including photoresist and developer application.

MEASURED RESULTS AND AMPLIFIER COMPARISON

Measured performance is shown in Figure 3. Small-signal gain generally exceeds 5 dB across 1 to 20 GHz. Output power at 1 dB gain compression exceeds 500 mW across most of the operating band, with power-added efficiency of 15 percent or greater. Input and output SWR is typically less than 2.25:1 from 2 to 20 GHz. These results demonstrate that efficient, high power distributed amplifier design using baseline production processes is feasible.

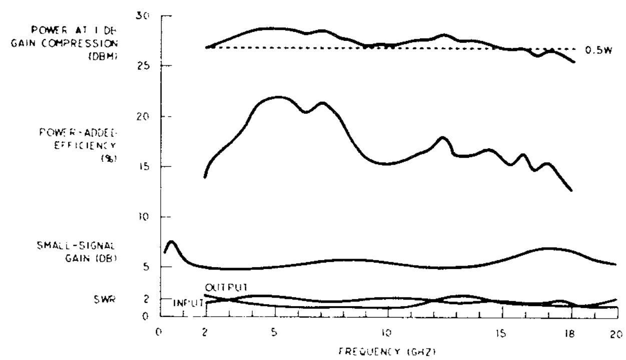


Figure 3. TGA8220 Distributed Amplifier RF Performance

Wideband distributed amplifiers are generally more performance tolerant to process variations than reactively-matched amplifiers. The TGA8014 is a 6 to 18 GHz lossy-reactive matched two-stage 0.4 W power amplifier [2]. Both MMICs are similar in size and have nearly the same total gate widths (2.0 mm) and overall complexity. Output power and power-added efficiency for both amplifiers are very similar. TGA8014 gain averages 8 dB versus 5 dB for the TGA8220, but the distributed amplifier in/out SWR and gain ripple are much lower. The TGA8014 circuit schematic is shown in Figure 4.

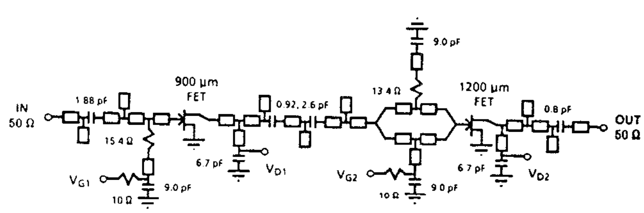
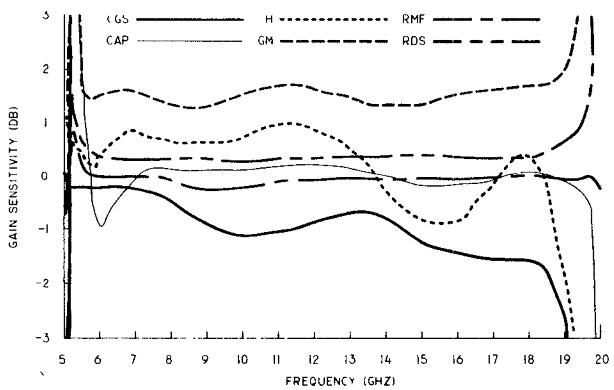


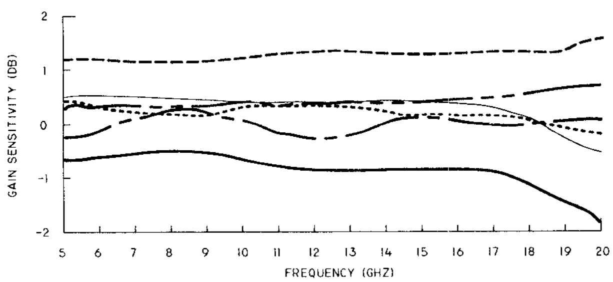
Figure 4. TGA8014 Schematic

Computed gain sensitivity matrices in dB format, which normalizes the sensitivities to the different gain levels, are plotted for the TGA8014 and TGA8220 in Figure 5. Component variables are FET transconductance, G_M; gate-source capacitance, C_{GS};

drain-source output resistance, R_{DS}; GaAs and metal film resistors, R_M or R_{MF}; MIM capacitance, CAP; and substrate height, H. To interpret the graphs, look at TGA8014 sensitivity at 11.5 GHz: a 10-percent increase in G_M will produce a 17-percent increase in gain (dB). In comparison, TGA8220 gain for this case will increase by only 12 percent. The sensitivity of the TGA8220 distributed amplifier to G_M, C_{GS} and substrate height variations is less than that of TGA8014. Since FET gain is most sensitive to G_M and C_{GS}, RF yield of TGA8220 to a given gain window specification will be higher than that of TGA8014. This has been confirmed by Monte Carlo RF yield analyses of both circuits to ± 10% gain windows (in dB) about the nominal gain, across 6 to 18 GHz. The same process distributions were used for both amplifiers in the analyses. Predicted yield to a gain window specification for the TGA8220 is nearly twice that of the TGA8014.



(a) TGA8014 A 6-18 GHz. Reactive-Lossy Matched Power Amplifier



(b) TGA8220 A 2-20 GHZ. Distributed Power Amplifier

Figure 5. Gain Sensitivity Matrices

CONCLUSION

A distributed power amplifier with state-of-the-art performance has been designed and demonstrated. By utilizing rigorous design, layout, and modeling techniques, desired results were achieved on the first pass without using sub-half-micron gate lengths or MBE, VPE, or MOCVD material.

ACKNOWLEDGEMENTS

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REFERENCES

1. B. Kim and H. Q. Tserng, "High Power Distributed Amplifier Using MBE Synthesized Material," IEEE 1985 Microwave and Millimeter-wave Monolithic Circuits Symposium Digest, pp. 35-37.

2. S. Nelson, et al., "Power Amplifier Leads MMIC Line," Microwaves & RF, December 1986, pp. 125-132.